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| half\_adder.vhd  library IEEE;  use IEEE.STD\_LOGIC\_1164.ALL;  use IEEE.STD\_LOGIC\_ARITH.ALL;  use IEEE.STD\_LOGIC\_UNSIGNED.ALL;  entity half\_adder is  port (a, b : in std\_logic;  s, c :out std\_logic);  end half\_adder;  architecture behavior of half\_adder is  begin  s <= a xor b;  c <= a and b;  end behavior; | full\_adder.vhd  library IEEE;  use IEEE.STD\_LOGIC\_1164.ALL;  use IEEE.STD\_LOGIC\_ARITH.ALL;  use IEEE.STD\_LOGIC\_UNSIGNED.ALL;  entity full\_adder is  port (a, b, cin : in std\_logic;  s, cout :out std\_logic);  end full\_adder;  architecture behavior of full\_adder is  component half\_adder  port (a, b : in std\_logic;  s, c :out std\_logic);  end component;    signal ara1,ara2,ara3:std\_logic;    begin  ha1:half\_adder port map(  a=>cin,  b=>ara1,  c=>ara3,  s=>s);  ha2:half\_adder port map(  a=>a,  b=>b,  c=>ara2,  s=>ara1);  cout<=ara2 or ara3;  end behavior; |